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SUPPORT AND SALES

AUSTRALIA
Patents Act 1990

PROVISIONAL SPECIFICATION

200390... filed 28th February 2003

Invention Title : **Non Volatile Memory Cell**

Applicant: **Griffith University**

Inventors: H Barry Harrison
Sima Dimitrijev

The invention is described in the following statement:

NON VOLATILE MEMORY CELL

This invention relates to a nonvolatile memory cell and In particular to a silicon carbide based memory cell.

Background to the invention

Random Access Memory devices are volatile in that power is needed to retain data indefinitely as compared to non volatile storage.

Flash memory provides the complementary functions in modern electronic systems. Flash memory uses a floating gate which is charged or discharged to change the logic state. The charge and discharge times are finite and the discharge is relatively slow. It is a read-only memory (ROM), because the information writing takes too long and is limited to a certain number of writing cycles, so it cannot be used for RAM applications. However, it provides a nonvolatile storage of the information, which is kept even when any power is disconnected from the memory cells. Flash memory is also dependent on processing and in practice there is a need to adjust for processing by having a micro processor on the same chip with built in corrections.

There have been attempts to form non volatile random access memory (NVRAM) devices - a memory cell with access characteristics of silicon RAMs and with retention times of silicon ROMs (flash memories) - and USA patent 6373095 is an example.

Another challenge in developing memory devices is to enable an increase in memory capacity, and one way of achieving this is to reduce the feature size (currently at $8F^2$). F is the *minimum feature* (the minimum line width that can be achieved by a certain technology), and $8F^2$ shows that the structure of state-of-the-art memory cells is such that every cell takes an area of $8F^2$. This challenge has been outlined by S.Okhonin, M. Nagoga, J.M. Sallese and P Fazan (IEEE Electron Device letters Vol 23 No 2 Feb 2002). A limiting factor in down scaling feature size in silicon is that memory capacitance is dependent on F.

Silicon Carbide is not widely used to produce semiconductor devices which are mostly fabricated in silicon. Silicon carbide has been proposed for use in

transistors but not for memory devices in USA patents 5831288, 6218254,and 6281521.

USA patent 6365919 discloses a Silicon carbide junction field effect transistor (JFET).

USA patent 5465249 discloses a silicon carbide NVRAM cell which incorporates a transistor and capacitor in silicon carbide. The memory elements are implemented in silicon carbide and the access transistor (switch) is in silicon. The memory cell is read by sensing capacitance

USA patents 5801401, 5989958 and 6166401 disclose a memory device using a silicon carbide floating gate.

It is an object of this invention to provide a NVRAM that is capable of having a small feature size and avoids the disadvantages of flash memory. A further object is to provide a cell that can enable more aggressive down scaling and significant reductions in power dissipation. This of course will also increase the density of memory storage.

Brief description of the invention

To this end the present invention provides a NVRAM which includes a silicon carbide transistor performing the role of a nonleaky switch and a memory transistor that can be implemented in either silicon or silicon carbide. The gate oxide of the silicon-carbide transistors is formed in the presence of NO or N_2O. This invention provides a silicon carbide transistor in which the mechanisms of electron-hole recombination (both, bulk and surface), as well as charge leakage, are reduced to sufficiently low levels that the transistor can be used as a nonleaky switch. When connected to the gate of a memory capacitor or transistor, the *off* mode of the nonleaky switch sets the gate of the memory element as a *floating gate* (in electrical terms). In general; it allows any terminal of a memory cell to be electrically disconnected so that non equilibrium charge can be maintained in the memory cell.

This invention is partly predicated on the realisation that nitrided oxide in the SiO_2 – SiC interface results in long charge retention times that makes it suitable

for accessing non volatile memory storage devices. The process of preparing the device is based on *nitridation* of the SiC-SiO_2 interface, either by a direct oxide growth (in) or oxide annealing in either NO or N_2O ambients.

In a further aspect of this invention there is provided a metal oxide semiconductor field effect transistor (MOSFET) implemented in silicon or silicon carbide with the bit lines (the MOSFET drains) crossing the word lines (the MOSFET sources) and the gates are in parallel with the word lines. This MOSFET acts as a single transistor (capacitor less) NVRAM cell. Preferably the writing operations are performed with grounded gates (zero gate-to-substrate voltage). The cell is read by sensing resistance. This has the consequence of enabling multiple levels with a consequential increase in memory capacity and and removes problems in down scaling the cell size.

This structure has a feature size of 4 F^2. Another advantage is that the logic levels are implemented as at least two states of channel resistance due to the channel charge and that the difference in the resistance values of the two levels is not critically dependent on F. A further advantage is multi level logic which is bought about by different amounts of channel charge and thus multiple levels of resistance.

Compared to Flash memory lower voltages are required and the speed of charging and discharging is greater than with Flash. The memory cell of this invention has none of the disadvantages of Flash memory with the added benefit that the cell may have several (infinite) logic states if they are needed.

This aspect of the invention is predicated on the use of a SiC-based switch (MOSFET) to connect the gates of the memory transistors, if a nonvolatile RAM is to be achieved. If the memory gates are connected by a switch that has relatively high leakage (for example, a silicon MOSFET), the storage time will not be practically infinite, although this implementation can enable valuable extensions of refresh times in modern dynamic RAMs.

The method for fabrication of SiC MOSFETs includes the essential step of forming a nitrided gate oxide and subsequently carrying out the ion implantation and then finishing the formation of the MOSFET. It is preferred to use self-aligned MOSFETs.

The fabrication method which results in a self aligned MOSFET with a metal gate provides performance improvements (better down scaling of F, reduced power consumption, and reduced leakage through the gate oxide). Self-aligned MOSFETs are routinely made in silicon (either with polysilicon or metal gates). The challenge in SiC is due to the need for high-temperature annealing to activate the doping of the drain and the source areas after creating them by ion implantation with the MOSFET gates as self-aligning masks. The ion implantation may be performed at room temperature, but this requires prohibitively high annealing temperatures (>1400^{0}C). An alternative method is to perform the ion-implantation at high temperatures (about 800^{0}C), in which case the post implant annealing temperature up to 1300^{0}C is sufficient. The challenge with this is to find a metal (or a metal-based structure) that will provide the necessary adhesion to the gate oxide and that will withstand the high-temperature ion implantation. A preferred metal is Molybdenum and this allows a Mo-gate process that satisfies the conditions for fabrication of self-aligned SiC MOSFETs by hot ion implantation. Other suitable materials are P^+ polysilicon, and platinum silicide. An essential feature of this preferred method is the use of a capping dielectric (deposited oxide, for example) to prevent sublimation of the Mo gate, as well as coating the capping dielectric by a thin metal film to avoid damaging charging effects during the ion implantation.

Detailed description of the invention

Preferred embodiments of the invention will be described with reference to the drawings in which

Figure 1 is cross sectional view of a memory cell of this invention;

Figure 2 is a top view of the cell of figure 1;

Figure 3 illustrates the reading states of the cell of this invention;

Figure 4 illustrates the writing of logic 0;

Figure 5 illustrates the writing of logic 1;

Figure 6 illustrates step 1 of a fabrication method applicable to this invention;

Figure 7 illustrates step 2 of a fabrication method applicable to this invention;

Figure 8 illustrates step 3 of a fabrication method applicable to this invention;

Figure 9 illustrates step 4 of a fabrication method applicable to this invention;
Figure 10 illustrates step 5 of a fabrication method applicable to this invention;
Figure 11 illustrates step 6 of a fabrication method applicable to this invention;
Figure 12 illustrates step 8 of a fabrication method applicable to this invention;

Technological Considerations

The critical technological aspects, in terms of proper functioning of the memory cell of this invention, are limited to the issues of (1) low recombination rate and (2) low leakage through the gate oxide. The requirement for low recombination rate is the reason why silicon cannot be used to achieve very long storage times. Many semiconductor materials with wide energy gaps can theoretically fulfill this requirement, at least as far as the bulk recombination rate is concerned. However, the difficulty lies in achieving a high quality interface between the semiconductor with wide energy gap and a dielectric, so that the surface recombination rate is sufficiently reduced. The native oxide of SiC is silicon-dioxide, the same dielectric as in the only industry-standard semiconductor-dielectric interface developed so far — the silicon–silicon dioxide interface. SiC is the only wide energy gap material that can provide a high-quality interface with its native dielectric, so the implementation of the nonleaky switch in this invention, is practically limited to silicon carbide substrate. There are many SiC polytypes (3C, 4H, 6H,...) and each of them would satisfy the essential requirements. The energy gap of 3C SiC is about 2.4 eV, which is a smaller value compared to the other common polytypes (about 3.0 eV for 6H and about 3.2 eV for 4H SiC). This means the recombination rate will be the largest of all common polytypes. However, a good-quality 3C material with a good quality gate-dielectric interface can provide a low enough recombination rate for the implementation of the nonvolatile RAMs . The attractiveness of 3C SiC is that it can be deposited on Si, enabling integration of the nonvolatile RAM with state-of-the-art complementary electronics and with the mature technology processes developed for silicon. The quality of the interface between SiC and the gate dielectric is essential for both requirements (low surface recombination rate and low leakage through the gate dielectric). This invention provides a specific treatment of the interface

between SiC and the gate dielectric as one means of achieving the required high-quality interface. This treatment results in "nitrided" interface, where nitrogen atoms remove and passivate interfacial defects. The interface nitridation can be achieved by either direct oxide growth or by annealing of pre-grown oxide in either NO or N_2O ambients at high temperatures (>1000^{0}C).

The memory cell of this invention stores minority carriers in the MOSFET channel (holes in the case of P-channel MOSFET on N-type substrate). Given that the memory MOSFETs share a common substrate and that all the MOSFETs along a word line will have connected gates, it is preferable to select the gate material so that the surface is not inverted at V_G = 0V. In other words, it is preferable to select the gate material so that the flat-band voltage (V_{FB}) is positive for a P-channel MOSFET. The flat-band voltage is given by

$$V_{FB} = \phi_{ms} - q\, N_{OC}/C_{ox}$$

where ϕ_{ms} is the work-function difference, N_{OC} is the density of the effective gate-oxide charge, and C_{ox} is the gate-oxide capacitance. In the case of N-type 4H SiC (P-channel MOSFETs), the condition for a positive flat-band voltage is satisfied by the most suitable gate materials. For example, the work-function differences are about 0.5 eV, 1.2 eV, and 1.8 eV for molybdenum, P^+ polysilicon, and platinum silicide, respectively. In the case of N-type 3C Si, the work-function differences are about -0.4 eV, 0.3 eV, and 0.8 eV for molybdenum, P^+ polysilicon, and platinum silicide, respectively. Given that the shift due to the effective oxide charge is usually negative ($- q\, N_{OC}/C_{ox}<0$), the preferred material in the case of 3C SiC is platinum silicide.

To reduce the surface recombination rate, the gate leakage, and the minimum feature (F), the preferred implementation of the MOSFET in this invention is as a self-aligned structure (self-aligned gate and source/drain regions). Self-aligned MOSFETs have been made in silicon (either with polysilicon or metal gates). The challenge in SiC is due to the need for high-temperature annealing to activate the doping of the drain and the source areas after creating them by ion implantation with the MOSFET gates as self-aligning masks. The ion implantation can be

performed at room temperature, but this requires prohibitively high annealing temperatures (>1400^{0}C). An alternative method is to perform the ion-implantation at high temperatures (about 800^{0}C), in which case the post implant annealing temperature up to 1300^{0}C is sufficient. Gate materials that satisfy this criterion include polysilicon, molybdenum, and platinum silicides.

A preferred memory cell is shown schematically in figures 1 and 2.
The cell topology is a capacitor-less 1T-DRAM cell . Fig. 1 shows the cross-section and Fig. 2 shows the top view. Technologically, the cell is an ordinary *metal–oxide–semiconductor field-effect transistor (MOSFET)*. If SiC MOSFET is used, the SiC film that is needed can be deposited on Si to allow an integration with today's Si electronics. As shown in Fig. 2, the bit lines (drains of the MOSFETs) cross the word lines (sources of the MOSFETs). The gates of the MOSFETs (labeled by G) run in parallel with the word lines (sources of the MOSFETs). This corresponds to a cell area of $4F^2$.

Fig. 1 illustrates the implementation with P-channel MOSFETs [current experimental results suggest lower recombination rates and leakage when the gate oxide (gate dielectric) is grown on N-type SiC (N substrate in Fig. 1)]. Further, a specific suggestion is to select the gate material so that the flat-band voltage $V_{FB}>0$ and the threshold voltage $V_T<0$. With this, the channel area is depleted for $V_G=0$. Some negative charge exists in the gate to compensate the positive donor ions in the depleted SiC surface, but this equilibrium charge will be neglected in the following considerations (for clarity). Note that fully analogous descriptions are valid if N-channel MOSFET is used.

Information Reading

The equilibrium state (depleted surface) corresponds to a very high channel resistance and is defined as logic '0' (Fig. 3a). The reading of this state is achieved by connecting the word line to ground and the bit line to a small negative voltage (V_B). The channel-resistance at the cross between the word and the bit lines determines the current, and if this MOSFET has a depleted channel, there is no current (logic '0').

The logic '1' state is achieved by trapping extra negative charge in the floating gate to reduce the potential in the channel sufficiently so that the inversion layer of holes is formed at the SiC surface (Fig. 3b). Reading is the same, with a difference that the response is a significant current through the channel (logic '1'). Note that the application of voltage to the drains and the grounding of the sources does not affect the stored information. There will be a small alteration of the surface potential, but the charge in the floating gate will not change, so the surface SiC condition will be restored after the reading cycle.

Storage Time

The logic '1' state is nonequilibrium, so the natural mechanisms will act to remove the inversion-layer holes to bring the structure into equilibrium. There are two possible mechanisms of hole removal: (1) leakage through the gate oxide (gate dielectric), and (2) leakage through the switch in the connecting circuit. A high-quality oxide-SiC interface can be achieved to reduce the leakage to sufficient levels. Experimental results indicate that sufficiently low bulk and surface-recombination levels are possible to achieve a practically nonleaky switch (implemented as a SiC MOSFET).

Connecting the Floating Gate for the Writing Operations

Writing operations (for both, logic '1' and logic '0') are performed with grounded gates. Therefore, the use of "floating" gates in this invention is quite different from the use of floating gates in today's flash memories (ROMs). In this invention, the gates are electrically disconnected from ground, by using a SiC MOSFET as a switch, to enable straightforward selection of a cell for information reading and writing. It has been already described that the trapped charge in the floating gate restores the state of the cell after the disturbance caused by the V_B potential used for information reading. Likewise, the state of a cell is not altered when a bit line (MOSFET drains) is connected to a potential for the purpose of information writing, as will be described in the following text.

Writing Logic '0'

Logic '0' corresponds to the equilibrium state (depleted surface). To set this state, the gate line along a selected word line is grounded (Fig. 4). Importantly, this does not change the state of any of the connected MOSFETs that may be in

logic '1' state, as the logic '1' states were also written with the gates grounded. After this, the corresponding bit line is grounded, closing a ground-to-ground circuit through the gate-channel capacitance of the MOSFET in the cross between the word and the gate lines. This removes the holes from the channel.

Writing Logic '1'

Again, the gate line along a selected word line is grounded first. In this case, however, the word line (sources) is not left disconnected, but is connected to a positive voltage that is just bellow the forward-bias voltage of the source–substrate P–N junction. This leads to a small increase in the density of electrons in the gate, but there should be no injection of holes by the source, so that the original state of the depleted surface is restored in the logic '0' MOSFETs that are not selected by the bit line (drains disconnected). Explained in another way, the positive threshold-voltage shift due to the source-to-substrate bias ("inverted body effect") should be limited so that the threshold voltage remains negative and no holes are induced in the channel. A sufficiently large negative voltage is applied to the selected bit line (MOSFET drains) so that source–substrate P–N junction of the selected MOSFET is set in forward-bias mode and a current of holes flows through the channel. Note that the existence of holes in the channel means that the threshold voltage is shifted to a positive value by the drain bias. As the channel holes induce electrons in the gate (Fig. 5), the gate is disconnected to trap the electrons (the situation of a floating gate charged with extra electrons). A simpler procedure for writing the logic '1' state is possible if the inverted body effect in a given MOSFET is strong enough to shift the threshold voltage from negative to positive values by itself. In that case, the drain-to-gate circuit has to be used for writing, given that the drain and gate lines cross each other enabling the selection of a single MOSFET. Therefore, after the gate is grounded, a sufficiently high drain voltage is applied to shift the threshold voltage to positive values (again, the drain voltage should not be higher than the turn-on voltage of the drain-to-substrate diode). Given that the gate-to-substrate voltage is zero, the channel of holes is formed, increasing the gate capacitance to its inversion level and increasing the negative charge in the gate.

N-Channel Inversion Type Self-aligned MOSFET Fabrication Steps:

The following describe in detail the fabrication processes for n-channel inversion type self-aligned MOSFET.

1] Define Active Region: see figure 6

1.1. Clean wafer
1.2. Sputtered 500-nm thick field oxide - SiO_2 [3 hrs = 1.1um]
1.3. Deposit photoresist & soft bake
1.4. Expose UV (mask 1)
1.5. Develop photoresist & hard bake
1.6. Etch field oxide with BHF
1.7. Remove photoresist by ethanol

2] Grown Gate Oxide: see figure 7

2.1. Clean wafer (without HF)***
2.2. Thermally grown 50 nm gate oxide (nitrided oxide)
[1hr NO, 4hrO_2, 2hrNO, and cool down overnight]

3] Formation of Metal Contact Layer for Gate Oxide: see figure 8

3.1. Sputtered 1-um thick Mo [200W for 55 min]
3.2. Deposit 200 nm SiO_2 by spin-on-glass (sog) [4000rpm]
3.3. Soft bake @ 200°C for 1 hr
3.4. Hard bake @ 900°C for 20 min.
3.5. Cool down to 700°C
3.6. Deposit photoresist & soft bake
3.7. Expose UV (mask 2)
3.8. Develop photoresist & hard bake
3.9. Etch SiO_2 (spin-on-glass) with BHF
3.10. Etch Mo [1 min 15s can etch 1-um thick Mo]

4] Ion Implantation (N^+): see figure 9

5] Activate & Drive-in implanted ion: see figure 10

5.1. Annealing at 950°C (or 1300°C) for 30 min

6] *Open Source/Drain windows:* see figure 11

6.1. Spin-on-glass, $SiO_{2(Mo)}$ (to protect Mo sidewall from Ni etchant)

6.2. Deposit photoresist & soft bake

6.3. Expose UV (mask 3)

6.4. Develop photoresist & hard bake

6.5. Etch SiO_2 ($SiO_{2(Mo)}$, spin-on-glass on MOS-C, MOSFET, and R_c test structure & nitrided oxide on R_c test structure) with BHF

6.6. Remove photoresist by etanol

7] *Prepare Bulk Contact Area:*

7.1. Deposit photoresist & soft bake

7.2. Expose UV (mask 4)

7.3. Develop photoresist & hard bake

7.4. Etch Mo

7.5. Etch nitirded oxide

8] *Metallization of Source/Drain/Bulk contact:* see figure 12

8.1. Sputtered 500 nm Ni (time = 40min @ 200°C)

8.2. Deposit photoresist & soft bake

8.3. Expose UV (mask 5)

8.4. Develop photoresist & hard bake

8.5. Etch Ni [Al etchant]

8.6. Remove photoresist

In summary, the present invention exploits low bulk and surface *recombination* rates that can be achieved in SiC. This fact is utilized to propose a nonvolatile dynamic random-access memory (DRAM) with the following features:

1. Practically indefinite information storage, even when no power is connected to the cell (memory).

2. Fast reading and writing — comparable to today's DRAMs on silicon that need refreshing (volatile DRAMs).
3. Indefinite number of writing cycles.
4. A smaller cell size than today's commercial volatile DRAMs — $4F^2$, where F is the minimum feature size.
5. Easier downscaling of F compared to today's volatile DRAMs. This is due to the following factors: (1) the '0' and '1' logic levels are implemented as two states of a channel resistance, so the difference between the two levels does not critically depend on how small F is (as opposed to this, a relatively small difference in two capacitance levels is used in today's volatile DRAMs, so that downscaling of the memory capacitor is already a limiting factor); (2) lack of any diffusion in SiC removes the most significant fabrication issues related to channel-length downscaling.
6. Reduced power dissipation.
7. Multiple logic levels and therefore the chance of higher memory capacities.
8. Full compatibility with silicon enable support electronics to be produced in this more mature material.
9. The higher thermal conductivity will also enable higher mass storage of digital information.etc.

Those skilled in the art will realize that the invention can be implemented in a variety of ways in a number of configurations without departing from the the critical teaching of this invention.

CLAIMS

1. NVRAM in which silicon or silicon-carbide transistors are used as memory elements and silicon-carbide transistors are used as switches connecting the memory elements, with the gate oxide of the silicon-carbide transistors being prepared by direct oxide growth or by annealing of pre-grown oxide in the presence of NO or N_2O.

2. A metal oxide semiconductor field effect transistor (MOSFET) implemented in silicon or silicon carbide with the bit lines (the MOSFET drains) crossing the word lines (the MOSFET sources) and the gates are in parallel with the word lines.

3. A MOSFET as claimed in claim 2 in which writing operations are performed with grounded gates.

4. An NVRAM as claimed in claim 1 in which the cell is read by sensing resistance

5. A method of fabricating an NVRAM as claimed in claim1 or a MOSFET as claimed in claim 2 which includes the step of forming a nitrided silicon oxide gate on the silicon carbide substrate and subsequently carrying out the ion implantation and then finishing the formation of the MOSFET.

6. NVRAM as claimed in claim 1 in which the transistor includes a gate and the gate material is selected from molybdenum, P^+ polysilicon, and platinum silicide.

7. NVRAM in which the electron-hole generation/recombination rate and charge leakage are reduced so much that a non-equilibrium charge can be maintained for substantial periods of time, which includes a silicon carbide transistor used as a switch to connect memory cells.

ABSTRACT

A non volatile random access memory cell is formed in silicon or silicon carbide and the gate oxide is formed or annealed in the presence of nitrogen. The memory cell comprises a metal oxide semiconductor field effect transistor (MOSFET) implemented in silicon or silicon carbide with the bit lines (the MOSFET drains) crossing the word lines (the MOSFET sources) and the gates are in parallel with the word lines. The gate of the MOSFET acts to store charge and thus dictate the "logical" state of the device. The memory cell is connected by silicon-carbide MOSFETs to prevent charge leakage. The fabrication method includes the step of forming a nitrided silicon oxide gate on the silicon carbide substrate and subsequently carrying out the ion implantation and then finishing the formation of a self aligned MOSFET.

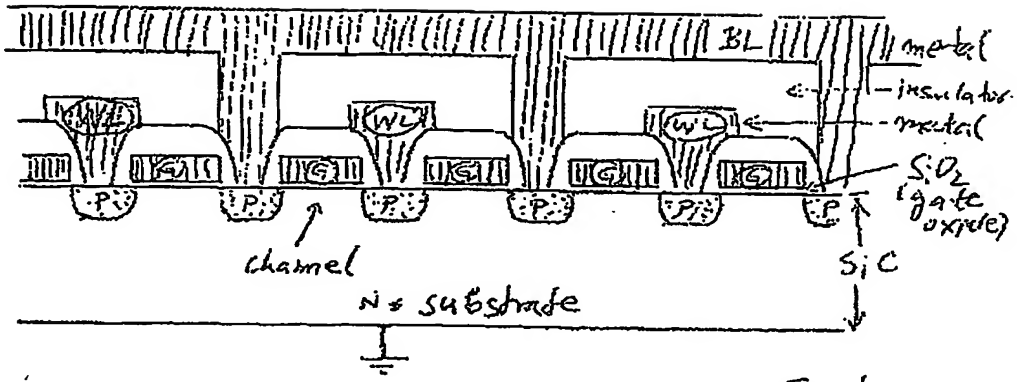
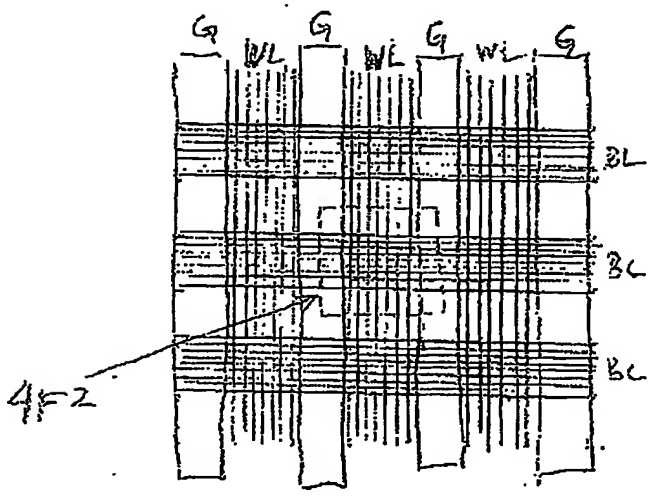

BL
metal
insulator
metal
WL
WL
WL
G
G
G
G
G
P
P
P
P
P
P
SiO_2
(gate oxide)
channel
Si C
N+ substrate

Fig. 1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G
WL
G
WL
G
BL
BL
BL
4F2

Fig. 2

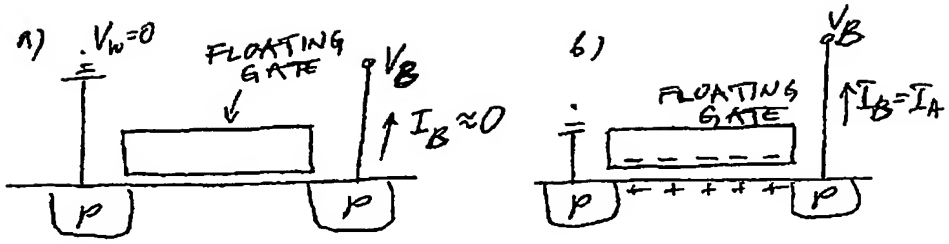

Fig. 3 Reading logic "0" (a) and logic "1" (b)

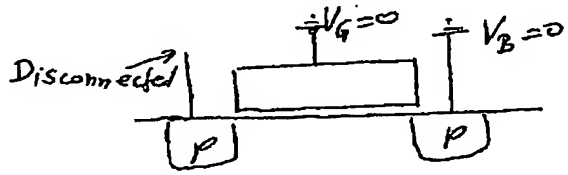

Fig. 4 Writing "0"

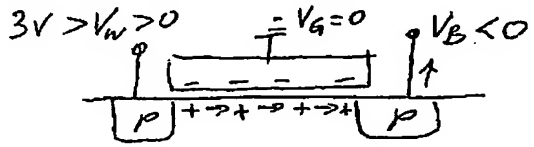

Fig. 5 Writing "1"

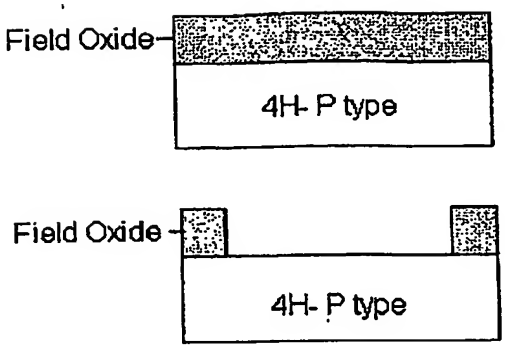

FIGURE 6

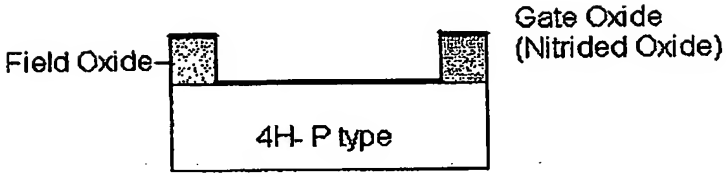

FIGURE 7

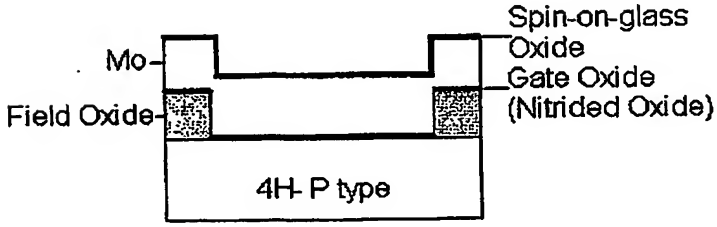

FIGURE 8

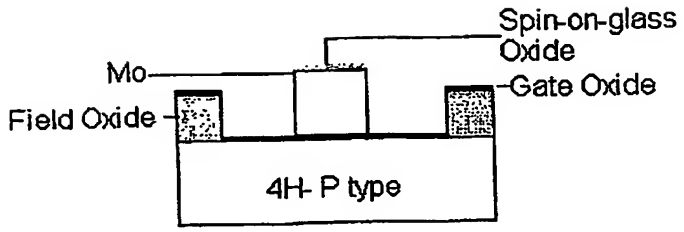

FIGURE 9

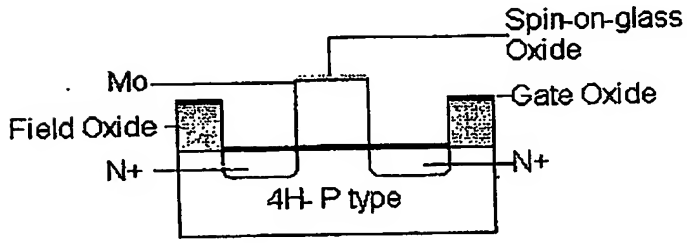

FIGURE 10

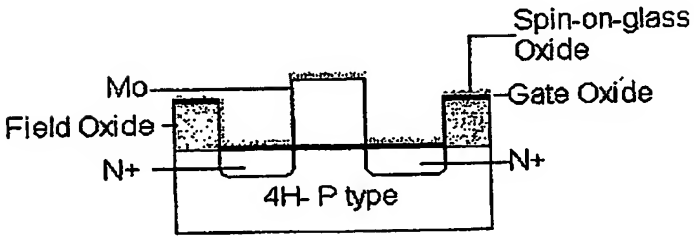

FIGURE 11

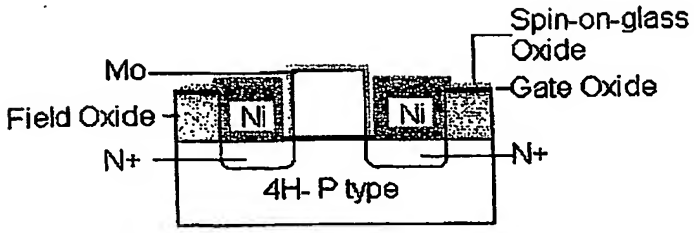
Spin-on-glass
Oxide
Mo
Gate Oxide
Field Oxide
Ni
Ni
N+
N+
4H- P type

FIGURE 12

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